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A 1GHZ CLASS E POWER AMPLIFIER FOR WIRELESS APPLICATIONS

R. SHANKAR[1], M. C. JOHN WISELIN[2], KANCHANA. D[3] & SREEJA. B. S[4]

[1]*Research Scholar, PRIST University, Thanjavur, Tamil Nadu, India*

[2]*Head and Professor, EEE, Vidya Academy of Science and Technology, Trivandrum, India*

[3,4]*Department of ECE, SSN College of Engineering, Chennai, Tamil Nadu, India*

ABSTRACT

In this paper, a class E power Amplifier (PA) suitable for wireless applications (Wi-Max, cellular phones, cordless phones etc,) is proposed by using the device of RF3931GaN HEMT (Gallium Nitrate High Electron Mobility Transistor).The proposed class E power Amplifier for achieving high output power and increasing gain up to 14.327dB and operates in the frequency range of 1GHz. The designed Power Added Efficiency (PAE) is 64% after optimization and the maximum source power achieved is 32dBw.

KEYWORDS: Class E Power Amplifier, Gain, Power Added Efficiency & Wireless Applications

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Original Article

I. INTRODUCTION

Wireless communication is the biggest research, have grown rapidly for recent years and they transfer their information from one point to another point, without any electrical wires. The wireless system is used for hospitals also, it makes the equipment smaller and easy way and it reduces the hazards also. Recent research for wireless application is headphones. Consumer demand requires the portable handset to be cheap and have minimum size and weight, as well as long battery life. The class E power amplifier is used to increase the high power efficiency and gain for increasing the usage of applications.

The power amplifier dominates that they have reduced the power consumption at the transmitter side, so that they achieve high power and high efficiency in the receiver end. The class E power amplifier is a single switch connection they have ON switch and OFF switch, the switches should be connected in the load network, because to reduce the power dissipation, if that decreases automatically, the output power should increase and also the efficiency and the main aim is to reduce the size by using the class E power amplifier, theoretically which gives 100% efficiency. This paper organized only the designs [1] process of operating maximum frequency for the dual band ratio of duty cycle 0.5 and the switching frequency of 0.1-10 GHz. Brama suggested that[2-4] integrating the high power CMOS process for the parallel circuit of power amplifier it offers low power dissipation it is used in DSP part and that achieves only 30.5dBm of source power and 48% of power added efficiency with the help of balun transceiver for low power integrated CMOS for short range applications off wireless field [5] designing the two class E power amplifier, one should be inverter and the rectifier for achieving high efficiency of the power is denoted in dc/dc converter [6] using the transmission lines designing the class E power amplifier [7] for the low power dc/dc power converter they achieved by 1GHz frequency range[8] by using the shunt capacitance for novel switching frequency operation for high power application for fewer usage the power efficiency is less [9] zigbee operates in three different application in the frequency range of 2.4 GHz is achieved [10-11] high efficiency for the

frequency range of 2.5 GHz and the switching frequency should maintained high and choosing the proper frequency reduces the size.

The reminder of the paper is organized as follows. Section 2 briefly discussed about the power amplifier. In Section3, class E power amplifier using RF3931 transistor is designed and simulated using ADS tool. Finally Section 4, Concludes the paper and discusses some future work.

II. POWER AMPLIFIER CIRCUIT

The power amplifier of RF having two ports input port and output port that should match each other in 1GHz the input port. From *Figure 1* input inductance (Lin) and capacitance (Cin) the input terminals should be in load network so that decreases the power losses.

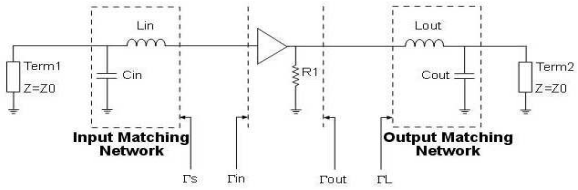

Figure 1: Proposed Power Amplifier

And then measuring the reflection coefficient in the source side that should match with the device used and the same thing the output match also done with inductance (Lout) and capacitance (Cout) with impedance value of 50 ohm and then matches the network and achieve the power added efficiency up to 64%. Then the RF3931 transistor is matched with matching network is used.

III. DESIGN AND SIMULTION

The general power amplifier having different procedure to design the first is DC load line analysis and then stability conditions of the device chosen, after that load pull analysis for achieving high gain then impedance matching for improving the power added efficiency.

DC Loadline Analysis

The DC load line analysis used for power consumption and load line is a graphical representation of non linear devices between the current and voltage and they shows different region. In *Figure 2* the RF3931 device is used and the IDS denotes the current of drain and source region and the VDS and VGS for measuring the voltage of the terminals by using the FET curve is used to measuring the dc load line.

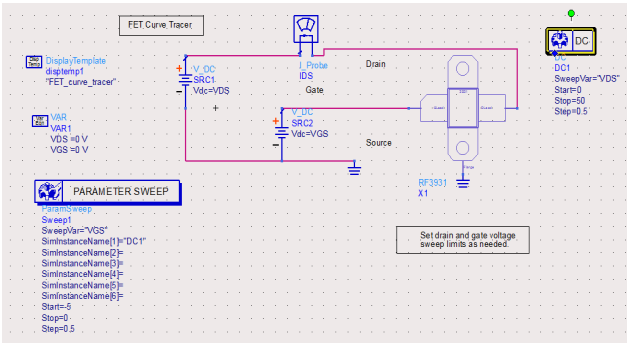

Figure 2: Schematic of DC Load Line Analysis

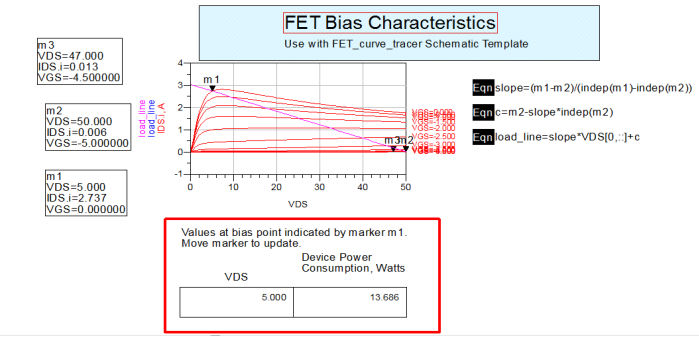

Figure 3: Results for Power Consumption

In *Figure 3* represents three different regions and load line analysis 1.Active Region denotes that have points in some particular region between the current and voltage that is the center point also called as operating point or Q-point are used to calculating slope equation between m1 and m2 marker and this case the transistor should in active region. 2. Saturation region denotes that they have maximum current and minimum voltage or zero voltage and this case the transistor should be in ON state. 3. Cutoff Region denotes having maximum voltage and zero current or vice versa for saturation region and then transistor should be in OFF state. From *Figure 3* says that m1 have VDS value of 5 and IDS value of 2.7 and m3 have VDS 47 and IDS -4.5 if increasing the voltage it will decrease the current and reduces the power consumption so easily used for wireless applications.

Bias and Stability

Biasing is used to determined the flow of current in the device and they have three terminals gate, drain, source

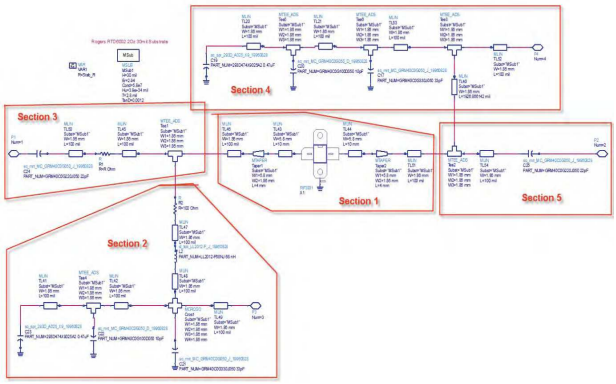

Figure 4: Bias and Stability

First the device should be placed in terminals as mentioned and then the section 2 is in gate side they have three bypass capacitor and DC bias choke (inductor) and resistors are connected for measuring the flow of current in bias region and section 3 is an input side of biasing device they connecting resistor for the stability of the device and achieve stability for power devices after that section 4 denotes that this part having bias network to drain terminals and section 5 for output device to identify whether the device is stable or unstable so that they can used for power amplifier design and the stability conditions are stability factor and measurement the factor measures the unity or greater than unity or one and then measurement for finding the accuracy of device values if that is not satisfies then the device should unstable that is oscillation state or negative resistance condition so generally biasing for reducing the errors in the device.

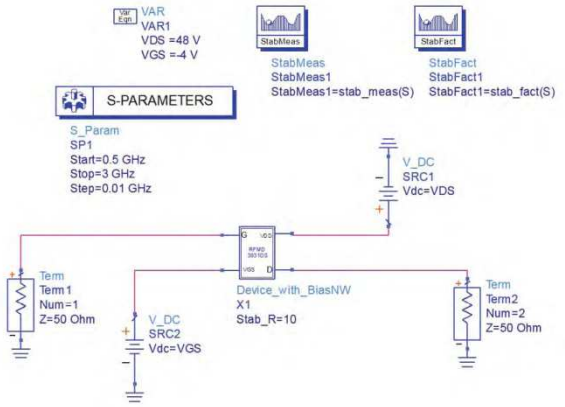

Figure 5: Symbol of Bias and Stability Conditions

From *Figure 5* mentioned the stability measurements and factors are in the tool itself and make different sections into small symbol that shows that they have RF as an input and RF output values and measuring the stability functions in it. From *Figure 6* represents the two conditions of stability is stability factor and measurements are satisfied.

Stability factor should be greater than one and stability measurement should be lesser than one are satisfied.

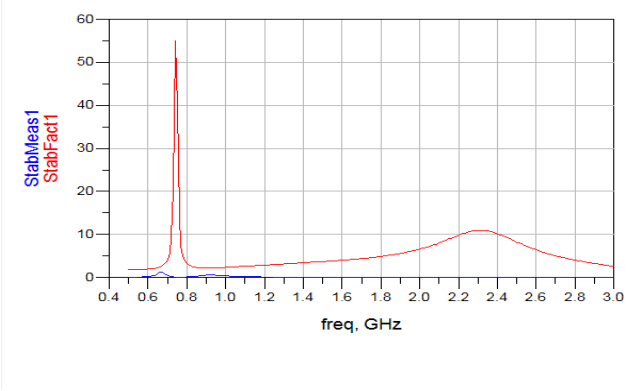

Figure 6: Achieved Stability Conditions

Load Pull Analysis

Generally load pull analysis for achieving the high output power and used to increasing the gain and source power the representation of load pull analysis is set of contour in smith chart and process of load pull analysis for measuring the input power by using the output and gain,

At the load gives maximum power and gain bias current at maximum power 0.795 and the gain of the maximum power is 10.483 and at the maximum power added efficiency is 44dB is achieved after changing the source power to 32dB then the gain has 14 dB is achieved. From *Figure 7* the load pull analysis can determined the one tone source is in build and then by using the symbol of bias and stability and the ground and drain connected to DC and VDS and VGS should connected to bias designed for 1000MHz. And finally achieving high gain and source power is shown in *Figure 8 and 9*.

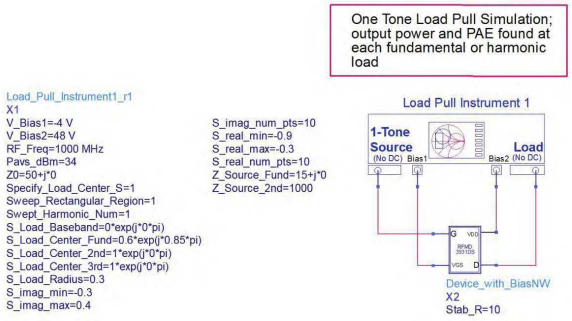

Figure 7: Schematic of Load Pull Analysis

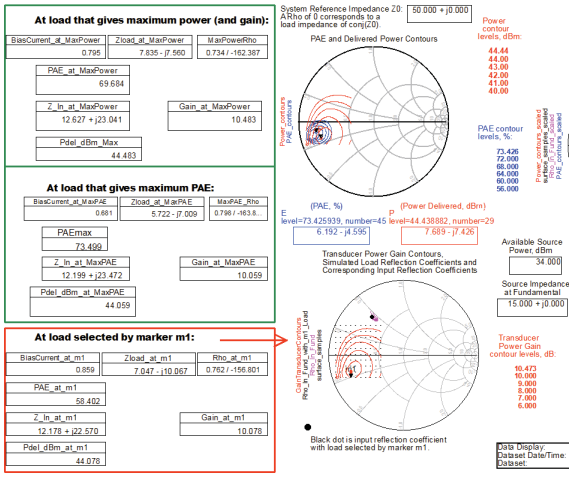

Figure 8: Complete Results of Load Pull

From *Figure 8* at load that gives maximum power (and gain) the Zload_at_MaxPower 7.835-j*7.560 equation for output port, the input designed by smith chart and then simulate for 1GHz. At load that gives maximum PAE the Z_in_at_MaxPAE gives 12.159+j*23.47 given for input port and then simulated by using the smith chart so by using the load pull analysis design the matching network. From *Figure 9* shows that achieving the high gain by changing the value of power source to 32dBm and then the gain values can change up to 14.327 dB.

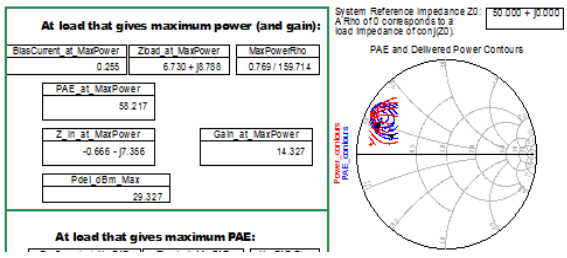

Figure 9: Achieving high gain at maximum power

Impedance Matching

Generally matching is to matches the two devices but in RF they have to match the two port devices that is the input and output port is designed and then matched for 1GHz design and then implemented from *Figure 10* the matching of input and output is shown. The device bias should be placed the input matching can designed by the value of load pull analysis of 12.6+j*23 for the input match and designed by using microstrip lines and scattering parameters and then make

it as a small symbol. The output matching also calculated by using the load pull analysis the value of Z_load is 7.835-j*7.56 value is designed and simulated by scattering parameters and then denotes the range and symbol can mentioned as output matching network, the process of matching network by using the device bias stab and two matching port can be used in it. From *Figure 10* showing the PAE for calculating the values of vin, vdc, vout and the harmonic balance (HB) used to measure the spectrum in frequency dB and the input is 32 before the optimization the PAE 32% and dBm(Vout) is 41.03 values.

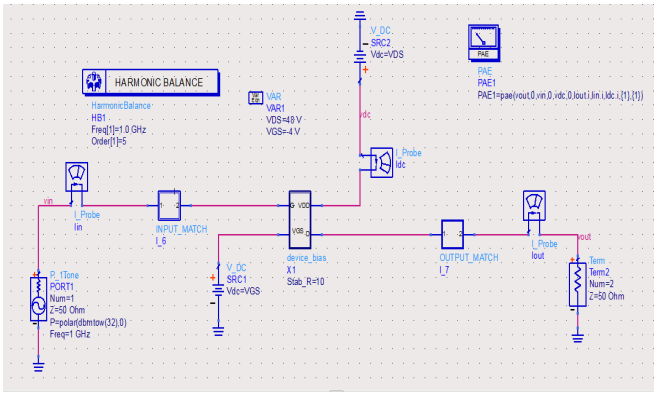

Figure 10: Design and Matching the Input and Output Port

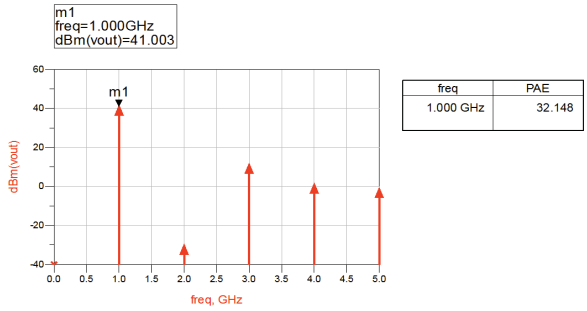

Figure 11: Results for Before Optimization Impedance Matching

In this case they have achieved only 32% of power added efficiency for 1GHz that is not enough for the wireless application and all other application so efficiency have to increase more by using the optimization. After optimization and tuning the two goals can be placed one should measure the vout and other should used for measure the frequency spectrum and the parameter sweep is used to measure the input power (pin) optimum should be done.

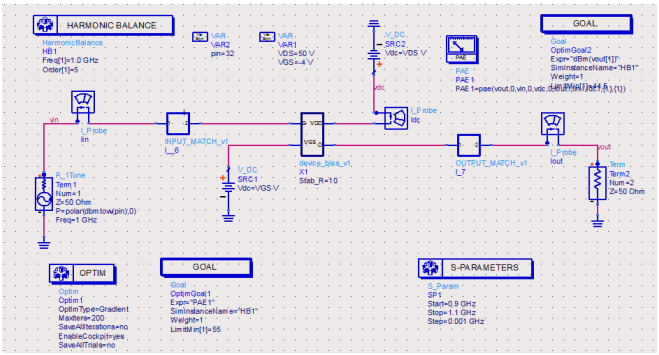

Figure 12: Schematic of Impedance Matching with Optimization Goal

The process of optimization is tuning values for achieving high efficiency and then increasing the values in *Figure*

13 shows frequency versus dBm (vout) the process of after optimization output is 44.501 and PAE is 64.650%.

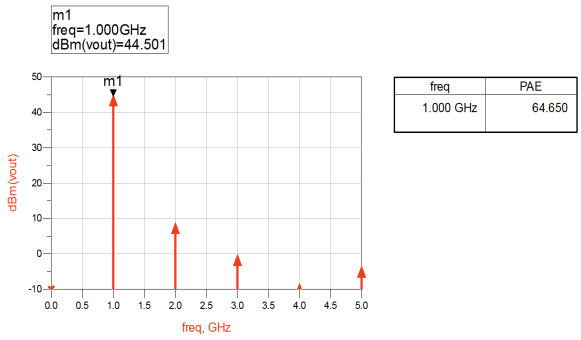

Figure 13: After Optimized Output

IV. CONCLUSIONS

This paper gives a broad review for class E power amplifier for the applications of wireless systems by using the RF3931 transistor device made by GaN HEMT and the operating frequency is 1GHz and achieving high gain of 14.37dB and also high efficiency is designed by using ADS tool. For future work design the power converter by using two class E amplifier.

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